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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,114	09/30/2003	Marcus W. May	SIG000090	4983

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EXAMINER	
LAXTON, GARY L	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 02/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/675,114	MAY, MARCUS W.
	Examiner	Art Unit
	Gary L. Laxton	2838

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4* is/are allowed.

6)☒ Claim(s) *5,6,11,12,17 and 18* is/are rejected.

7)☒ Claim(s) *7-10,13-16,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 12/05/2005 have been fully considered but they are not persuasive.

Applicant basically argues that Appeltans does not teach or suggest disabling the switching transistors as part of regulating the output voltage, but teaches changing states (i.e., changing the on time of the switching transistors 2 and 11) based on how the output voltage compares with a first or a second threshold voltage. Column 6 lines 37-39 and 43 disclose that Appeltans does indeed disable the transistors 2 and 11.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 5, 6, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Appeltans (US 5,552,694) in view of Bittner (US RE37,609).

Claims 5, 6, 17 and 18; Appeltans discloses a converter circuit to convert a battery voltage to an output voltage (col. 10 line 37), the converter circuit including a pair of switching transistors (2, 11) that switch alternately to have the battery voltage converted to produce the output voltage; and a control circuit to receive a feedback of the output voltage as part of a

voltage mode control loop to maintain the output voltage within a specified value, the control circuit including an upper limit level detect circuit and a lower limit level detect circuit to detect upper and lower limit levels for the output voltage (9); the control circuit uses pulse frequency modulation to control the output voltage; wherein when the output voltage is above the upper threshold, the control circuit reduces the switching frequency to a minimum frequency above the audible range (see also col.6 lines 37-39 and 43).

However, Appeltans does not disclose the control circuit disabling the converter circuit when the output voltage is at the upper limit level and to enable the converter circuit when the output voltage is at the lower limit level to maintain the output voltage between the upper and lower limit levels by use of the voltage mode control loop.

Bittner teaches a pulse frequency modulation control scheme that disables the converter when the output voltage rises above a threshold level and enables the converter when the output voltage is at a lower limit (col. 4 lines 7-44).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the pulse frequency modulation control circuit of Appeltans in order to disable the converter circuit when the output voltage is at the upper limit level and to enable the converter circuit when the output voltage is at the lower limit level to maintain the output voltage between the upper and lower limit levels by use of the voltage mode control loop as taught by Bittner to further reduce the switching losses of the converter circuit resulting from lowering the gate drive power dissipation of the switches in the PFM mode as taught by Bittner.

4. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Appeltans (US 5,552,694) in view of Malcolm et al (US 6,373,954) and Bittner (US RE37,609).

Appeltans disclose a converter circuit to convert the battery voltage to an output voltage, the converter circuit including a pair of switching transistors that switch alternately to have the battery voltage converted to produce the output voltage; and a control circuit to receive a feedback of the output voltage as part of a voltage mode control loop of the output voltage to maintain the output voltage within a specified value, the control circuit including an upper limit level detect circuit and a lower limit level detect circuit to detect upper and lower limit levels for the output voltage;

However, Appeltans does not disclose an integrated circuit which has an audio system integrated therein having an input interface; a digital signal processor; and an output amplifier; wherein the DC converter powers the digital signal processor and output amplifier and the control circuit to disable the converter circuit when the output voltage is at the upper limit level and to enable the converter circuit when the output voltage is at the lower limit level to maintain the output voltage between the upper and lower limit levels by use of the voltage mode control loop.

Malcolm et al teach an input interface to receive audio data input; a digital signal processor to receive the audio input and generate processed audio data; an output amplifier to output the processed audio data external to the integrated circuit. The circuit obviously requires power. DC power converter circuits obviously supply power.

Bittner teaches a control circuit that disables a converter circuit when the output voltage is at the upper limit level and enables the converter circuit when the output voltage is at the lower limit level to maintain the output voltage between the upper and lower limit levels by use of the voltage mode control loop (col. 4 lines 7-44)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the DC converter of Appeltans in an integrated audio system circuit as taught by Malcolm et al and to modify the control circuit of Appeltans in order to disable the converter circuit when the output voltage is at the upper limit level and to enable the converter circuit when the output voltage is at the lower limit level to maintain the output voltage between the upper and lower limit levels by use of the voltage mode control loop as taught by Bittner to further reduce the switching losses of the converter circuit resulting from lowering the gate drive power dissipation of the switches in the PFM mode as taught by Bittner. The control circuit of the DC-DC converter further includes a comparator (9) in the control loop to compare the output voltage to a reference value to detect a sign change at a crossover point, the sign change indicating when the 6utput voltage has reached the upper or lower limit levels and the sign change to be detected the upper and lower limit level detect circuits.

Allowable Subject Matter

5. Claims 1-4 are allowed.

6. Claims 7-10, 13-16, 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

Claims 1-4; prior art fails to disclose or suggest, inter alia, a pulse frequency modulation unit further including a filter to filter the feedback of the output voltage to detect sign changes at the filter when the upper and lower limit levels are detected and to skip a predetermined number of pulses from the filter after one of the sign changes to turn off the voltage converter.

Claims 7-10; prior art fails to disclose or suggest, inter alia, a filter to receive an output from the comparator to detect the sign change to identify when the upper or lower limit level is reached.

Claims 13-16; prior art fails to disclose or suggest, inter alia, a DC-DC converter further including a high rate filter and a low rate filter to filter the output from the comparator to control switching operation of the pair of switching transistors, but only the high rate filter is used to generate a control signal to enable and disable the pair of transistors

Claims 19 and 20; prior art fails to disclose or suggest, inter alia, a method to provide a voltage mode control loop in a DC/DC converter that further includes filtering to detect the sign change when one of the limit levels is reached to generate a control signal to enable and disable the pair of transistors.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,396,251 Corva et al disclose a control circuit to receive a feedback voltage; the control circuit including an upper limit level detect circuit and a lower limit level detect circuit to detect upper and lower limit levels for the output voltage; the control circuit disables the converter circuit when the output voltage is at the upper limit level and to enables the converter circuit when the output voltage is at the lower limit level to maintain the output voltage between the upper and lower limit levels by use of a voltage mode control loop (col. 5 lines 50-55).

US 6,965,221 Lipcsei et al disclose a feedback voltage; the control circuit including an upper limit level detect circuit and a lower limit level detect circuit to detect upper and lower limit levels for the output voltage; the control circuit disables the converter circuit when the output voltage is at the upper limit level and to enables the converter circuit when the output voltage is at the lower limit level to maintain the output voltage between the upper and lower limit levels by use of a voltage mode control loop (fig 1B)

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

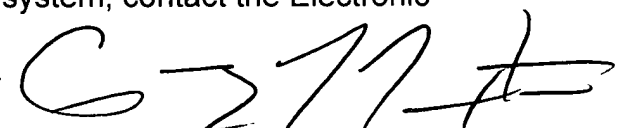
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (571) 272-2079. The examiner can normally be reached on Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Karl Easthom can be reached on (571) 272-1989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Gary L. Laxton
Primary Examiner
Art Unit 2838

1/26/2006